In the Claims:

1. (Currently amended) A radiation-emitting thin-film semiconductor chip with an epitaxial multilayer structure ~~(12)~~, which contains an active, radiation-generating layer ~~(14)~~ and has a first main face ~~(16)~~ and a second main face ~~(18)~~ - remote from the first main face - for coupling out the radiation generated in the active, radiation-generating layer,

~~characterized in that~~ wherein

the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ is coupled to a reflective layer or interface, and ~~the~~ a region ~~(22)~~ of the multilayer structure that adjoins the second main face ~~(18)~~ of the multilayer structure is patterned one- or two-dimensionally.

2. (Currently amended) The semiconductor chip as claimed in claim 1,

~~characterized in that~~ wherein

a carrier element is coupled to the first main face ~~(16)~~ and the reflective layer or interface is arranged between the carrier element and the multilayer structure.

3. (Currently amended) The semiconductor chip as claimed in claim 1 ~~or 2~~,

~~characterized in that~~ wherein

the region ~~(22)~~ of the multilayer structure that adjoins the second main face ~~(18)~~ of the multilayer structure ~~(12)~~ has convex elevations ~~(26).~~

4. (Currently amended) The semiconductor chip as claimed in claim 3,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have the form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

5. (Currently amended) The semiconductor chip as claimed in claim 3,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have the form of cones or a triangular cross-sectional form.

6. (Currently amended) The semiconductor chip as claimed in claim 3,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have the form of sphere segments or a circle segment cross-sectional form.

7. (Currently amended) The semiconductor chip as claimed in claim 3 ~~one of claims 3 to 6~~,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have an inclination angle (β) of between approximately 30° and approximately 70°.

8. (Currently amended) The semiconductor chip as claimed in claim 7,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have an inclination angle (β) of between approximately 40° and approximately 50°.

9. (Currently amended) The semiconductor chip as claimed in claim 3 ~~one of claims 3 to 8~~,

~~characterized in that~~ wherein

the height (h1) of the elevations ~~(26)~~ is at least as large as the distance (h2) between a non-patterned region ~~(20)~~ of the multilayer structure ~~(12)~~ and the active, radiation-generating layer ~~(14).~~

10. (Currently amended) The semiconductor chip as claimed in claim 9,

~~characterized in that~~ wherein

the height (h1) of the elevations ~~(26)~~ is approximately twice as large as the distance (h2) between the non-patterned region ~~(20)~~ of the multilayer structure and the active, radiation-generating layer.

11. (Currently amended) The semiconductor chip as claimed in claim 3 ~~one of claims 3 to 10~~,

~~characterized in that~~ wherein

a cell size (d) of the elevations ~~(26)~~ is at most approximately five times as large as the height (h1) of the elevations.

12. (Currently amended) The semiconductor chip as claimed in claim 11,

~~characterized in that~~ wherein

the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

13. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 12~~,

~~characterized in that~~ wherein

the layer ~~(28)~~ or interface coupled to the first main area ~~(16)~~ of the multilayer structure ~~(12)~~ has a reflectivity of at least 70%.

14. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 12~~,

~~characterized in that~~ wherein

the layer ~~(28)~~ or interface coupled to the first main area ~~(16)~~ of the multilayer structure ~~(12)~~ has a reflectivity of at least 85%.

15. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 14~~,

~~characterized in that~~ wherein

the multilayer structure ~~(12)~~ is applied on a carrier substrate ~~(30)~~ either directly by its first main face ~~(16)~~ or via a reflective layer ~~(28)~~.

16. (Currently amended) The semiconductor chip as claimed in claim 15,

~~characterized in that~~ wherein

the reflective layer or the carrier substrate simultaneously serves as a contact layer of the semiconductor chip.

17. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 16~~,

~~characterized in that~~ wherein

a conductive, transparent layer is applied on the second main face ~~(18)~~ of the multilayer structure ~~(12)~~.

18. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 17~~,

~~characterized in that~~ wherein

a transparent protective layer ~~(32)~~ is applied on the second main face ~~(18)~~ of the multilayer structure ~~(12)~~.

19. (Currently amended) A radiation-emitting thin-film semiconductor chip with an epitaxial multilayer structure ~~(12)~~, which contains an active, radiation-generating layer ~~(14)~~ and has a first main face ~~(16)~~ and a second main face ~~(18)~~ - remote from the first main face - for coupling out the radiation generated in the active, radiation-generating layer,

~~characterized in that~~ wherein

the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ is coupled to a reflective layer ~~(28)~~ or interface, and a transparent layer ~~(34)~~ is provided between the first main face ~~(16)~~ of the multilayer structure and the reflective layer or interface, said transparent layer being patterned one- or two-dimensionally.

20. (Currently amended) The semiconductor chip as claimed in claim 19,

~~characterized in that~~ wherein

the transparent layer ~~(34)~~ is conductive.

21. (Currently amended) The semiconductor chip as claimed in claim 19 ~~or 20~~,

~~characterized in that~~ wherein

the transparent layer ~~(34)~~ between the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ and the reflective layer ~~(28)~~ or interface has convex elevations ~~(26')~~.

22. (Currently amended) The semiconductor chip as claimed in claim 21,

~~characterized in that~~ wherein

the elevations ~~(26')~~ have the form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

23. (Currently amended) The semiconductor chip as claimed in claim 21 ~~or 22~~, ~~characterized in that~~ wherein

the elevations ~~(26')~~ have an inclination angle (β) of between approximately 30° and approximately 70°.

24. (Currently amended) The semiconductor chip as claimed in claim 21 ~~or 22~~, ~~characterized in that~~ wherein

the elevations ~~(26')~~ have an inclination angle (β) of between approximately 40° and approximately 50°.

25. (Currently amended) The semiconductor chip as claimed in claim 21 ~~one of claims 21 to 24~~, ~~characterized in that~~ wherein

the height (h1) of the elevations ~~(26')~~ is at least as large as the height (h2) of a non-patterned region ~~(35)~~ of the multilayer structure ~~(12)~~ between the active, radiation-generating layer ~~(14)~~ and the elevations.

26. (Currently amended) The semiconductor chip as claimed in claim 25, ~~characterized in that~~ wherein

the height (h1) of the elevations ~~(26')~~ is approximately twice as large as the height (h2) of the non-patterned region ~~(35)~~ of the multilayer structure between the active, radiation-generating layer and the elevations.

27. (Currently amended) The semiconductor chip as claimed in claim 21 ~~one of claims 21 to 26~~,

~~characterized in that~~ wherein

a cell size (d) of the elevations ~~(26')~~ is at most approximately five times as large as the height (h1) of the elevations.

28. (Currently amended) The semiconductor chip as claimed in claim 27,

~~characterized in that~~ wherein

the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

29. (Currently amended) The semiconductor chip as claimed in claim 19 ~~one of claims 19 to 28~~,

~~characterized in that~~ wherein

the layer or interface coupled to the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ has a reflectivity of at least 70%.

30. The semiconductor chip as claimed in claim 29,

~~characterized in that~~ wherein

the layer or interface coupled to the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ has a reflectivity of at least 85%.

31. (Currently amended) The semiconductor chip as claimed in claim 19 ~~one of claims 19 to 30~~,

~~characterized in that~~ wherein

the reflective layer ~~(28)~~ is applied on a carrier substrate ~~(30)~~ or the reflective interface is formed by a carrier substrate ~~(30)~~.

32. (Currently amended) The semiconductor chip as claimed in claim 31,

~~characterized in that~~ wherein

the reflective layer or the carrier substrate simultaneously serves as a contact layer of the semiconductor chip.

33. The semiconductor chip as claimed in claim 19 ~~one of claims 19 to 32~~,

~~characterized in that~~ wherein

a transparent protective layer is applied on the second main face ~~(18)~~ of the multilayer structure ~~(12)~~.

34. (Currently amended) A radiation-emitting thin-film semiconductor chip with an epitaxial multilayer structure ~~(12)~~, which contains an active, radiation-generating layer (14) and has a first main face ~~(16)~~ and a second main face ~~(18)~~ - remote from the first main face - for coupling out the radiation generated in the active, radiation-generating layer,

~~characterized in that~~ wherein

the first main face ~~(16)~~ of the multilayer structure ~~(12)~~ is coupled to a reflective layer or interface, and a one- or two-dimensionally patterned coating layer ~~(32, 38)~~ is arranged on the second main face ~~(18)~~ of the multilayer structure ~~(12)~~.

35. (Currently amended) The semiconductor chip as claimed in claim 34, ~~characterized in that~~ wherein

the coating layer ~~(32, 38)~~ has convex elevations ~~(36)~~.

36. (Currently amended) The semiconductor chip as claimed in claim 34 ~~or 35~~, ~~characterized in that~~ wherein

the coating layer ~~(32, 38)~~ is transparent and conductive.

37. (Currently amended) The semiconductor chip as claimed in claim 34 ~~one of claims 34 to 36~~, ~~characterized in that~~ wherein

a metal layer is arranged between the coating layer ~~(32, 38)~~ and the multilayer structure ~~(12)~~.

38. (Currently amended) The semiconductor chip as claimed in claim 37, ~~characterized in that~~ wherein

the metal layer is formed such that it is very thin or not closed, in particular in reticulated or insular fashion.

39. (Currently amended) The semiconductor chip as claimed in claim 34 ~~one of claims 34 to 38~~,

~~characterized in that~~ wherein

the elevations ~~(26)~~ have the form of pyramids, truncated pyramids, cones or truncated cones or a trapezoidal cross-sectional form or a triangular cross-sectional form or a circle-segment cross-sectional form.

40. (Currently amended) The semiconductor chip as claimed in claim 34 ~~one of claims 34 to 39~~,

~~characterized in that~~ wherein

the coating layer ~~(32, 38)~~ is formed in reticulated or insular fashion.

41. (Currently amended) The semiconductor chip as claimed in claim 1 ~~one of claims 1 to 40~~,

~~characterized in that~~ wherein

the multilayer structure ~~(12)~~ contains a material or a plurality of different materials based on GaN.

42. (New) The semiconductor chip as claimed in claim 19,

wherein

the multilayer structure contains a material or a plurality of different materials based on GaN.

43. (New) The semiconductor chip as claimed in claim 34,

wherein

the multilayer structure contains a material or a plurality of different materials based on GaN.